

WHAT IS CLAIMED IS:

1. A switch for switching packets from a plurality of sources comprising:

a memory in which portions of packets are stored; and

a transferring mechanism which transfers predetermined portions of a packet to the memory as the predetermined portions are received.

2. A switch as described in Claim 1 wherein the transferring mechanism transfers predetermined portions of the packet as fixed length segments as the fixed length segments are received followed by a single final segment of any length wherein the packet is transferred to the memory.

3. A switch as described in Claim 2 wherein the transferring mechanism transfers fixed length segments of different packets interleaved among each other as they are received to the memory.

4. A switch as described in Claim 3 wherein the transferring mechanism includes an aggregator which receives portions of packets from the plurality of sources.

5. A switch as described in Claim 4 wherein the memory includes a memory controller.

6. A switch as described in Claim 5 wherein the aggregator uses TDM to multiplex segments of packets from different sources to the memory controller.

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7. A switch as described in Claim 6 wherein the aggregator places an identifier with each segment identifying from which source the segments came from.

8. A switch as described in Claim 7 wherein the memory controller includes per source queues, and stores each segment in a corresponding per source queue based on the identifier of the segment.

9. A switch as described in Claim 8 wherein the memory controller includes per destination queues, and once all segments for a packet are received at a per source queue, all the segments of the packet are changed to a corresponding per destination queue.

10. A switch as described in Claim 9 wherein the memory controller has acceptance criteria for accepting segments, and if the segment is not accepted, then all previously received segments associated with the segment not accepted are purged from the per source queue and any segments associated with the segment not accepted that are received after the segment that was not accepted was received, are ignored.

11. A switch as described in Claim 10 including a fabric in which the aggregator and the memory controller are disposed, and including a separator disposed in the fabric connected to the aggregator.

12. A switch as described in Claim 11 including a port card having a striper which sends portions of packets to the aggregator, and an unstriper which receives portions of packets from the separator.

14. A method for switching packets comprising the steps  
of:

transferring predetermined portions of the packet to a memory of the switch as the predetermined portions are received at the transferring mechanism.

16. A method as described in Claim 15 wherein the transferring step includes the step of transferring fixed length segments of different packets as they are received interleaved among each other to the memory.

18. A method as described in Claim 17 wherein the transferring step includes the step of multiplexing with the

aggregator segments of packets from different sources to the memory controller.

19. A method as described in Claim 18 wherein before the transferring step, there is the step of placing by the aggregator an identifier with each segment identifying from which source the segment came from.

20. A method as described in Claim 19 wherein after the transferring step, there is the step of storing each segment in a corresponding per source queue of the memory controller based on the identifier of the segment.

21. A method as described in Claim 20 including after the storing step, there is the step of changing all segments of the packet in the source queue to a corresponding per destination queue of the memory controller once all the segments of the packet are received at the per source queue.

22. A method as described in Claim 21 wherein the receiving step includes the steps of purging all previously received segments associated with an unaccepted segment that does not meet acceptance criteria for accepting a segment of the memory controller, and ignoring all segments associated with the unaccepted segment received at the memory controller after the unaccepted segment is received at the memory controller.

23. A method as described in Claim 22 wherein the receiving step includes the step of receiving portions of packets from different sources at the aggregator of the transferring mechanism disposed in the fabric of the switch from a striper of a port card of the switch.

24. A method as described in Claim 23 including after the moving step, there is the step of sending portions of packets from the memory controller with a separator of the fabric to an ~~unstriper of the port card.~~

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